Amendments to and Listing of the Claims:

Please amend claims 1-3, 7 and 10, cancel claims 4-6 and add new claim 22, so that the claims read as follows:

1. (Currently Amended) A method of forming a polysilicon layer in a semiconductor device, comprising:

providing a substrate;

forming an oxide layer over the substrate;

depositing a first silicon layer over the oxide layer, wherein the first silicon layer comprises microcrystalline polysilicon, wherein the step of depositing a first silicon layer is performed with a low pressure chemical vapor deposition in the presence of a reactive gas containing silicon and a carrier gas, and wherein the reactive gas containing silicon is selected from the group consisting of SiH_4, SiH_2Cl_2, SiD_4, SiD_2Cl_2, $SiDCl_3$, $SiHCl_3$, SiD_3Cl, and SiH_3Cl;

depositing an amorphous silicon layer over the first silicon layer; and

annealing the amorphous silicon layer to form a polysilicon layer.

2. (Currently Amended) The method as claimed in claim 1, wherein the step of ~~forming~~ depositing a first silicon layer is performed at a furnace temperature of about 500°C to 700°C.

3. ((Currently Amended) The method as claimed in claim 1, wherein the step of ~~forming~~ depositing a first silicon layer is performed at a furnace pressure between about 0.2 m torr and 5 torr.

4-6. (Cancelled)

7. (Currently Amended) The method as claimed in claim [[6]] 22, wherein the flow rate of the carrier gas is about 100 sccm to 5,000 sccm.

8. (Original) The method as claimed in claim 1, wherein the first silicon layer has a thickness of about 50 to 2,000 angstroms.

9. (Original) The method as claimed in claim 1, wherein the amorphous silicon layer has a thickness of about 100 to 2,000 angstroms.

10. (Currently Amended) A method of forming a flash memory cell, comprising:

providing a substrate;

forming an oxide layer over the substrate;

forming a polysilicon floating gate over the oxide layer including

providing a bottom seed layer having microcrystalline polysilicon,

providing an upper amorphous silicon layer over the bottom seed layer,

and

annealing the upper amorphous silicon layer;

providing an inter-poly dielectric layer over the polysilicon floating gate; and

forming a polysilicon control gate over the inter-poly dielectric layer.

11. (Original) The method as claimed in claim 10, wherein the step of providing a bottom seed layer is performed at a furnace temperature of about 500°C to 700°C.

12. (Original) The method as claimed in claim 10, wherein the step of providing a bottom seed layer is performed with a single wafer low pressure chemical vapor deposition at a chamber temperature of about 650°C to 750°C.

13. (Original) The method as claimed in claim 10, wherein the step of providing a bottom seed layer is performed at a furnace pressure of between about 0.2 m torr and 5 torr.

14. (Original) The method as claimed in claim 10, wherein the step of providing a bottom seed layer is performed with a single wafer low pressure chemical vapor deposition at a pressure of about 50 torr to 500 torr.

15. (Original) The method as claimed in claim 10, wherein the deposition of the bottom seed layer is performed with a low pressure chemical vapor deposition in the presence of a reactive gas containing silicon and a carrier gas.

16. (Original) The method as claimed in claim 15, wherein the reactive gas containing silicon is selected from the group consisting of SiH_4, SiH_2Cl_2, SiD_4, SiD_2Cl_2, $SiDCI_3$, $SiHCI_3$, SiD_3CI, and SiH_3CI.

17. (Original) The method as claimed in claim 16, wherein the flow rate of the reactive gas containing silicon is about 20 sccm to 1,600 sccm.

18. (Original) The method as claimed in claim 15, wherein the carrier gas is selected from the group consisting of H_2, D_2 and D_3.

19. (Original) The method as claimed in claim 18, wherein the flow rate of the carrier gas is about 100 sccm to 5,000 sccm.

20. (Original) The method as claimed in claim 10, wherein the bottom seed layer has a thickness of about 50 to 2,000 angstroms.

21. (Original) The method as claimed in claim 10, wherein the upper amorphous silicon layer has a thickness of about 100 to 2,000 angstroms.

22. (New) A method of forming a polysilicon layer in a semiconductor device, comprising:

providing a substrate;

forming an oxide layer over the substrate;

depositing a first silicon layer over the oxide layer, wherein the first silicon layer comprises microcrystalline polysilicon, wherein the step of depositing a first silicon layer is performed with a lower pressure chemical vapor deposition in the presence of a reactive gas

containing silicon and a carrier gas, and wherein the carrier gas is selected from the group consisting of H_2, D_2 and D_3;

depositing an amorphous silicon layer over the first silicon layer; and

annealing the amorphous silicon layer to form a polysilicon layer.